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REMARKS

Claims 1-4, and 10-12 are pending in the present application. Applicants have amended claims 1 and 10. Claims 1-4, and 10-12 remain pending in the present application.

Amended Claims

Claims 1 and 10 have been amended to clarify the present invention. In particular, claims 1 and 10 have been amended to recite a method for manufacturing a memory device "on a silicon substrate" including the steps of providing a dual gate oxide in the core area, "wherein the dual gate oxide in the core area forms an interface between the oxide and the silicon substrate" and "strengthening the interface by providing a nitrification process in both the core area and periphery area . . . thereby improving the reliability of the dual gate oxide in the core area." Support for this amendment is found in the Specification at page 2, lines 9-11, and page 5, line 19 to page 6, line 1. No new matter has been presented. Moreover, because the amendments to claims 1 and 10 are clarifying amendments, the scopes of claims 1 and 10 are unchanged.

35 U.S.C. §103 Rejection

Claim 1 was rejected under 35 U.S.C. §103(a) as being unpatentable over Cappelletti et al. (U.S. Patent No. 5,637,520) in view of Nakata (U.S. Patent No. 5,254,489). Claims 2 and 10 were rejected as being unpatentable over Cappelletti in view of Nakata and further in view of Lee (U.S. Patent No. 5,175,120). Finally, claims 3, 4, 11 and 12 were rejected as being unpatentable over Cappelletti, Nakata, and Lee, and further in view of Chien et al. (U.S. Patent No. 6,436,759). In rejecting claim 1, the Examiner stated:

> Cappelletti et al. shows the invention substantially as claimed including a method comprising the steps of: providing a portion 35' of a dual gate oxide in a periphery area of the memory cell; simultaneously providing a dual gate oxide 61

in a core area of the memory device and completing the dual gate oxide 35" in the periphery area (see Figures 10-12 and column 4-lines 20-65).

Cappelletti et al. fails to expressly disclose providing a nitridation process in both the core area and periphery area of the memory device.

Nakata discloses forming an oxide film and subsequently performing a nitridation process and forming different films of different thickness for forming different MOS elements (see column 3, lines 51-58). In view of this disclosure, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the process of Cappelletti et al. so as to include an additional nitridation process after forming the oxides because the nitridation allows for a gate film of longer endurance.

Applicants respectfully disagree.

The present invention is directed to a method of manufacturing a flash memory device on a silicon substrate. In a conventional fabrication process, a gate oxide in the core area is nitrified in order to introduce nitrogen to the $Si\text{-}SiO_2$ interface, which in turn improves the reliability of the core gate oxide. During the nitrification process, however, the periphery area is also exposed to the nitrogen. The presence of nitrogen in the periphery area inhibits the growth of oxide. Therefore, forming a dual gate oxide in the periphery area is problematic.

The present invention addresses this problem by performing the nitrification process after the gate oxides in both the core area and in the periphery area have been formed. Nitrogen contamination in the periphery area is eliminated because the gate oxide has already been provided, and reliability of the flash memory device is improved.

The present invention, as recited in independent claim 1, provides:

1. A method for fabricating a memory device on a silicon substrate, the method comprising the steps of:

(a) providing a portion of a dual gate oxide in a periphery area of the memory device;

(b) simultaneously providing a dual gate oxide in a core area of the memory device and completing the dual gate oxide in the periphery area, wherein the dual gate oxide in the core area forms an interface between the oxide and the silicon substrate; and

(c) strengthening the interface by providing a nitrification process in

both the core area and periphery area of the memory device subsequent to steps (a) and (b), thereby improving the reliability of the dual gate oxide in the core area.

Independent claim 10 is a method claim reciting additional manufacturing steps subsequent to the strengthening step (c).

Cappelletti is directed to a process for fabricating a flash memory device. In the process, a gate oxide (35') in the periphery area (40a') is formed (FIG. 11), and then a gate oxide (61) is formed in the core area (40b') (FIG. 12). While the core gate oxide is formed (61), the thickness of periphery gate oxide 35" increases slightly to its final thickness (See FIG. 12). Thus, the thickness of the periphery gate oxide 35" is different from the thickness of the core gate oxide 61. After the gate oxide has been formed, conventional fabrication techniques are performed to produce the flash memory device.

Nakata is directed to a method for forming a first gate oxide having a different thickness than a second gate oxide. In one embodiment of Nakata, a first oxide layer (3) is formed over a substrate (FIG. 3A) and a portion of the first layer (3) is etched (FIG. 3B). Then a second oxide layer (5) is formed on the etched portion of the substrate, while the remaining portion of the first layer (3a) increases in thickness (FIG. 3C). At this time, the entire surface is nitrified (FIG. 3D) and a portion of the nitrified oxide is etched (FIG. 3E). Next, a third oxide layer (9) is formed on the etched portion of the substrate, while the remaining nitrified portions of the first (6) and second (7) layers maintain their respective thicknesses (FIG. 3F). By nitrifying the oxide layer, the thickness of the nitrified oxide layer is set and will not increase in a subsequent thermal oxidation step.

The combination of Cappelletti and Nakata teaches a method for manufacturing a flash memory device where the gate oxides in the periphery and core areas are formed using the method taught in Nakata. Specifically, referring to Cappelletti's Figure 12, an oxide layer is

grown in the periphery (40a') and core (40b') areas to a thickness equal to the final periphery gate oxide thickness (35"), and then nitrified. Next, the nitrified oxide in the core area (40b') is etched, and a new core gate oxide (61) is grown. The nitrified oxide layer (35") in the periphery (40a') retains its thickness. In the alternative, the oxide layer can be grown to a thickness equal to the final core gate oxide thickness (61), nitrified, and the nitrified oxide in the periphery area (40a') etched. Then a new periphery gate oxide (35") is grown and the nitrified oxide layer (61) in the core (40b') retains its thickness.

The combination of Cappelletti and Nakata fails to teach or suggest the cooperation of elements recited in claims 1 and 10. In particular, the combination fails to teach or suggest "providing *a portion* of a dual gate oxide in a periphery area," and then "*simultaneously* providing a dual gate oxide in a core area . . . and *completing* the dual gate oxide in the periphery area," as recited in claims 1 and 10. In Cappelletti in view of Nakata, one gate oxide is formed and nitrified *before* the other gate oxide is formed. Thus, the *completion* of any one gate oxide cannot occur *simultaneously* with the *formation* of another gate oxide.

Moreover, nothing in Cappelletti or Nakata mentions or suggests nitrifying an oxide layer for the purpose of "strengthening the [Si-SiO_2] interface by providing a nitrification process in both the core area and periphery area of the memory device *subsequent to*" providing a gate oxide in the core area and completing the gate oxide in the periphery, and "improving the reliability of the core gate oxide," as recited in claims 1 and 10. In the present invention, nitrification of the gate oxide in the core area introduces nitrogen to the Si-SiO_2 interface. The nitrogen strengthens the interface by bonding with the Si substrate. The nitrogen fortified interface is less susceptible to degradation during subsequent read, write and erase operations, thereby improving the reliability of the core gate oxide and the flash memory device.

In contrast, the nitrification process in Nakata is used to inhibit the growth of an oxide

layer in a subsequent thermal oxide treatment. Accordingly, the *combination* of Cappelletti and Nakata teaches nitrifying the oxide layer *prior to* completing either the core gate oxide or the periphery gate oxide. Nitrifying the oxide layer after completing both the core and periphery gate oxide would serve no purpose because the respective thicknesses of the *completed* gate oxide layers in the core and periphery areas would not need to be fixed. Applying Nakata's nitrification process at this stage in the manufacturing process would be pointless, and one skilled in the art would not be motivated to perform such an additional process step.

Accordingly, Applicants respectfully submit that there simply is no teaching or suggestion in Cappelletti and Nakata for "strengthening the [Si-SiO_2] interface by providing a nitrification process in both the core area and periphery area of the memory device *subsequent to*" "simultaneously providing a dual gate oxide in a core area . . . and completing the dual gate oxide in the periphery area," as recited in claims 1 and 10. Thus, claims 1 and 10 are allowable over the cited references.

Claims 2 and 10 were rejected as being unpatentable over Cappelletti in view of Nakata and further in view of Lee (U.S. Patent No. 5,175,120). Claim 2 depends on claim 1 and the above arguments apply with full force to that claim.

Claim 2 recites:

> 2. The method of claim 1 further comprising:
> (d)depositing a layer of type 1 polysilicon in both the core area and periphery area of the memory device;
> (e)depositing a layer of oxide nitride oxide over the layer of type-1 polysilicon; and
> (f)removing the layer of oxide nitride oxide and a portion of the layer of type-1 polysilicon from the periphery area of the memory device.

Claim 10 recites the same processing steps.

Lee is directed to a method for fabricating a memory device. Lee teaches, among other things, depositing a first layer of poly 1 (24) over a gate oxide layer 22, depositing an ONO layer

26 over the poly 1 layer 24, and then etching away from the periphery 14 the ONO layer 26 and poly 1 layer 24. Thereafter, a second layer of polysilicon 32 is deposited to cover the periphery 14 and core 12 areas. (Col. 3, lines 20-35; FIGS 1A, 1B, 2B).

The combination of Cappelletti, Nakata and Lee fails to teach or suggest the cooperation of elements recited in claims 2 and 10. Specifically, the combination fails to teach or suggest "removing . . . *a portion* of the layer of type-1 polysilicon from the periphery area of the memory device," as recited in claims 2 and 10. In Lee, the entire poly 1 layer 24 is etched away. (Col. 3, line 26-28; FIG. 2B).

Moreover, Lee fails to correct the deficiencies of Cappelletti in view of Nakata in that Lee also fails to teach or suggest the cooperation of elements recited in claims 1 and 10. In particular, Lee fails to teach or suggest "providing a portion of a dual gate oxide in a periphery area," "simultaneously providing a dual gate oxide in a core area . . . and completing the dual gate oxide in the periphery area," and then "strengthening the [Si-SiO_2] interface by providing a nitrification process in both the core area and periphery area of the memory device *subsequent to*" "simultaneously providing a dual gate oxide in a core area . . . and completing the dual gate oxide in the periphery area," as recited in claims 1 and 10. Accordingly, for the reasons stated above, claims 2 and 10 are allowable over the cited references.

Finally, claims 3, 4, 11 and 12 were rejected as being unpatentable over Cappelletti, Nakata, and Lee, and further in view of Chien et al. (U.S. Patent No. 6,436,759). Claims 3, 4, 11 and 12 depend on claims 1 and 10, respectively, and therefore the arguments pertaining to claims 1 and 10 apply with full force to claims 3, 4, 11 and 12. In rejecting these claims, the Examiner stated:

> Cappelletti et al., Nakata, and Lee are applied as above but fail to expressly disclose removing approximately half of the first polysilicon layer from the periphery layer.

Chien et al. discloses removing half of a first polysilicon layer from a gate 78 formed in the peripheral area 64 (see Figure 14 and column 4, lines 30-56).

Applicants respectfully submit that Chien is not prior art to the present invention because Chien's filing date post dates the filing date of the present invention. The present invention is a divisional application of a parent application filed June 15, 2000. Chien's filing dated is January 19, 2001. Accordingly, Chien cannot be a prior art reference to the present invention.

Cappelleti, Nakata and Lee do not teach or suggest the elements recited in claims 3, 4, 11 and 12. Therefore, Applicants respectfully submit that claims 3, 4, 11 and 12 are allowable over the cited references.

Conclusion

In view of the foregoing, it is submitted that the claims in the application are patentable over the cited references and are in condition for allowance. Reconsideration of the rejections and objections is requested.

Attached hereto and captioned "**Version with Markings to Show Changes Made**" is a marked-up version of the changes made to the claims by the current amendment.

Applicant's attorney believes this application in condition for allowance. Should any unresolved issues remain, Examiner is invited to call Applicant's attorney at the telephone number indicated below.

Respectfully submitted,

December 10, 2002
Date

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VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE CLAIMS:

1. (Amended) A method for fabricating a memory device on a silicon substrate, the method comprising the steps of:

(a) providing a portion of a dual gate oxide in a periphery area of the memory device;

(b) simultaneously providing a dual gate oxide in a core area of the memory device and completing the dual gate oxide in the periphery area, wherein the dual gate oxide in the core area forms an interface between the oxide and the silicon substrate; and

(c) strengthening the interface by providing a ~~nitridation~~ nitrification process in both the core area and periphery area of the memory device subsequent to steps (a) and (b), thereby improving the reliability of the dual gate oxide in the core area.

10. (Amended) A method for fabricating a memory device on a silicon substrate, the method comprising the steps of:

(a) providing a portion of a dual gate oxide in a periphery area of the memory device;

(b) simultaneously providing a dual gate oxide in a core area of the memory device and completing the dual gate oxide in the periphery area, wherein the dual gate oxide in the core area forms an interface between the oxide and the silicon substrate;

~~(c) strengthening the interface by providing a nitridation~~ nitrification process in both the core area and periphery area of the memory device subsequent to steps (a) and (b), thereby improving the reliability of the dual gate oxide in the core area;

~~(d)~~ depositing a layer of type-1 polysilicon in both the core area and periphery area of the memory device;

(e) depositing a layer of oxide nitride oxide over the layer of type-1 polysilicon; and

(f) removing the layer of oxide nitride oxide and a portion of the layer of type-1 polysilicon from the periphery area of the memory device.